Office Action Summary	Application No.	Applicant(s)	
	10/622,417	MAS ET AL.	
	Examiner	Art Unit	
	Joni Hsu	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 30-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5 and 30-45* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 6, 2007 has been entered.

Response to Arguments

2. Applicant's arguments filed August 6, 2007 with respect to Claims 1, 2, 4, 5, and 42-45 have been fully considered but they are not persuasive.

3. As per Claim 1, Applicant argues in Wu's (US006414689B1) device there is direct correspondence between displayed image and the image stored in the frame memory, and their positions are not offset relative to one another. Therefore, although addresses are accessed using an offset value instead of the full address, the address locations that are accessed remain the same, and correspond directly to the displayed image. By contrast, Claim 1 recites "activating pixels of a screen line associated with said address offset by a same pixel position offset value." Wu's device displays the image in the same way that it is stored in the frame memory (p. 7).

In reply, the Examiner points out that Claim 1 does not explicitly recite that the "pixel position offset value" is referring to the offset between the displayed image and the image stored in the frame memory. Therefore, this limitation is interpreted to mean that each screen line is offset from the prior screen line by the "same pixel position offset value", and "same" is interpreted to mean that the offset value itself remains constant. Wu teaches that the row address

of the frame memory for each screen line is offset from the prior screen line by a same constant offset value, and this is done by activating the pixels of the screen line associated with the address offset by a same pixel position offset value, based on the read states of the row associated with address (c. 9, ll. 11-45). So, Wu teaches this limitation as it is recited in Claim 1.

4. As per Claim 2, Applicant argues Wu does not teach a dedicated address circuit receiving the address of the row read by the read means and transmitting to the row driver a new address corresponding to the address of the read row offset by a same pixel position offset value for the same reasons given in the above discussion with respect to Claim 1 (p. 7).

In reply, the Examiner disagrees for the same reasons given above.

5. As per Claim 42, Applicant argues that the references relied upon do not teach a logic unit that receives a first row address corresponding to a row of the image data and performs an operation on the first row address using the row offset value to determine a second row address that is offset from the first row address (p. 8).

In reply, Examiner disagrees. Choi (US 20030076332A1), which was relied upon previously, teaches this limitation, as discussed below.

6. Applicant's arguments with respect to claims 30-41 have been considered but are moot in view of the new ground(s) of rejection.

7. As per Claim 30, Applicant argues references relied upon do not suggest second memory shifts storage locations at which the row of image data is stored based on the column offset value such that the row of image data is stored in second storage locations of the second memory, the second storage locations being shifted with respect to the first storage locations (p. 8).

In reply, new grounds of rejection are made in view of Miyachi (US006937224B1).

Claim Rejections - 35 USC § 102

8. The text of those sections of Title 35, U.S. Code 102(e) not included in this action can be found in a prior Office action.

9. Claims 30, 35, and 37 are rejected under 35 U.S.C. 102(e) as being anticipated by Miyachi (US006937224B1).

10. As per Claim 30, Miyachi teaches supplying select signal to nth row line and also supplying the data signal to the column lines, thereby displaying image to pixels located at intersecting points between nth row line and individual column lines (c. 3, ll. 58-63); and then iterating the display operation based on the data signal (shifting the column) while sequentially shifting row line to which the select signal is supplied (c. 4, ll. 4-7), which causes the position of the displayed image to be shifted. Therefore, Miyachi discloses a circuit for shifting a position at which an image is to be displayed, the image being represented by image data comprising a plurality of rows and a plurality of columns corresponding to pixels of the image (c. 3, ll. 58-63; c. 4, ll. 4-7), the circuit comprising a first memory (sampling memory 2, Fig. 31) that stores the image data; a second memory (holding memory 3) that receives a row of the image data from the first memory (2) and stores the row of image data at first storage locations of the second memory (3) (c. 1, ll. 12-20); and a control circuit (display control section) that provides a column offset value to the second memory (3); wherein the second memory (3) shifts storage locations at which the row of image data is stored based on the column offset value such that the row of image data is stored in second storage locations of the second memory (3), the second storage locations being shifted with respect to the first storage locations (c. 5, ll. 50-58; c. 6, ll. 1-7; c. 1, ll. 12-20; *supplying the data signal to the column lines, thereby displaying an image based on the*

data signal to pixels located at intersecting points between the nth row line and the individual column lines, iterating the image display operation based on the data signal while sequentially shifting the row line to which the select signal is supplied, c. 3, ll. 46-c. 4, ll. 7).

11. As per Claim 35, Miyachi teaches a plurality of column drivers (12, Fig. 1) that receive the row of image data from the second memory (holding memory 32, Fig. 2) (c. 12, ll. 22-36).

12. With regard to Claim 37, Miyachi teaches the second storage (holding memory) locations are offset from the first storage (sampling memory) locations by the column offset value (c. 1, ll. 12-20; c. 3, ll. 46-c. 4, ll. 7; c. 5, ll. 50-58; c. 6, ll. 1-7).

13. Thus, it reasonably appears that Miyachi describes or discloses every element of Claims 30, 35, and 37, and therefore anticipates the claims subject.

14. Claims 42-45 are rejected under 35 U.S.C. 102(e) as being anticipated by Choi (US0020030076332A1).

15. As per Claim 42, Choi teaches moving the image, and the movement order of the image is set as left, upper, right and lower directions, and the image is moved by one pixel in each of the directions [0036]. Therefore, Choi teaches a circuit for shifting a position at which an image is to be displayed, the image being represented by image data comprising a plurality of rows and a plurality of columns corresponding to pixels of the image. The circuit comprises a first memory (102, Fig. 1) that stores the image data [0031]; a logic unit (105); and a control circuit (104) that provides a row offset value to the logic unit [0036]. If the control circuit judges that the same image is displayed for a certain period of time, it sends the control signal, which causes the displayed image to move by one pixel in the left direction (row offset value), to the logic circuit [0035, 0036]. The logic circuit operates the display unit so that the image signal

transmitted can be displayed on a desired position of the display unit according to the control signal transmitted by the control circuit [0041]. Since the display is shifted after the same image is displayed, this means that the logic unit previously received a first row address corresponding to a row of image data for the image that was previously displayed. So, logic unit receives first row address corresponding to a row of image data and performs operation on first row address using row offset value to determine second row address that is offset from first row address.

16. As per Claim 43, Choi discloses that the control circuit (104, Fig. 1) further provides a row address offset direction to the logic unit (105) [0036, 0038].

17. As per Claim 44, Choi teaches that the position is determined by moving the image by one pixel in the left direction (row offset value) [0036, 0041]. Therefore, the position is determined by adding one pixel in the left direction to the previous position. Therefore, the second row address is determined by adding the row offset value to the first row address or subtracting the row offset value from the first row address.

18. As per Claim 45, Choi discloses that the control circuit provides a cyclic succession of row offset values to the logic unit [0036-0040].

19. Thus, it reasonably appears that Choi describes or discloses every element of Claims 42-45 and therefore anticipates the claims subject.

Claim Rejections - 35 USC § 103

20. The text of those sections of Title 35, U.S. Code 103(a) not included in this action can be found in a prior Office action.

21. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Richards (US006756976B2) in view of Glennon (US006359654B1), further in view of Wu (US006414689B1).

Richards describes a method for displaying an image by activation of pixels of an array screen based on an image stored in digital form in memory point rows of a frame memory, comprising a normal display mode comprising, for the display of a frame, the steps of: (a) providing a succession of row addresses associated with rows of the frame memory (310, Fig. 2a) (c. 5, ll. 65-c. 6, ll. 4; c. 13, ll. 45-51); (b) successively reading the states of memory points of the rows associated with the row addresses (c. 5, ll. 65-c. 6, ll. 4; c. 2, ll. 43-48); and (c) activating, for each row address, pixels of a line associated with the row address based on the read states of the row associated with the address (c. 2, ll. 43-48), further comprising a stand-by mode comprising replacing step (c) with the steps of: (d) providing, by a dedicated circuit (500, Fig. 15), a cyclic succession of offset values (c. 11, ll. 29-50; c. 13, ll. 52-67).

However, Richards does not teach cyclic succession of offset values is provided at frequency proportional to display frequency. But, Glennon teaches cyclic succession of offset values is provided at frequency proportional to display frequency (c. 3, ll. 51-65; c. 3, ll. 30-33).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Richards so the cyclic succession of offset values is provided at frequency proportional to display frequency as suggested by Glennon because Glennon suggests this is needed in order to achieve appearance of smooth motion (c. 3, ll. 66-c. 4, ll. 3).

However, Richards and Glennon do not teach (e) for each row address of frame memory, activating pixels of screen line associated with address offset by same pixel position offset value,

based on read states of the row associated with address. Claim 1 does not explicitly recite that the "pixel position offset value" is referring to the offset between the displayed image and the image stored in the frame memory. Therefore, this limitation is interpreted to mean that each screen line is offset from the prior screen line by the "same pixel position offset value", and "same" is interpreted to mean that the offset value itself remains constant. Wu teaches that the row address of the frame memory for each screen line is offset from the prior screen line by a same constant offset value, and this is done by (e) for each row address of frame memory, activating pixels of screen line associated with address offset by same pixel position offset value, based on read states of row associated with address (c. 9, ll. 11-45).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the devices of Richards and Glennon so that (e) for each row address of the frame memory, activating pixels of a screen line associated with the address offset by a same pixel position offset value, based on the read states of the row associated with the address as suggested by Wu because Wu suggests that computing the address slows down processing speed and increases power consumption (c. 2, ll. 19-24), and so obtaining address by address offsets (c. 3, ll. 1-9) increases processing speed and decreases power consumption (c. 2, ll, 32-36).

22. Claims 2, 4, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Richards (US006756976B2) in view of Glennon (US006359654B1), further in view of Leung (US005900887A), further in view of Wu (US006414689B1).

23. As per Claim 2, Richards describes a device for displaying an image on an array screen comprising a frame memory (310, Fig. 2a) comprising memory points arranged in rows and in columns (c. 5, ll. 61-65; c. 13, ll. 45-51; c. 17, ll. 47-49); a write means for storing in the frame

memory an image in digital form (c. 2, ll. 43-48; c. 3, ll. 4-6); a read means for reading the states of the memory points of a row of the frame memory at a determined row address (c. 3, ll. 39-42); a row driver (402, Fig. 3) for selecting a screen LINE based on the determined row address (c. 3, ll. 31-34); and a column driver for activating pixels of the selected line based on the states of memory points read by the read means, further comprising a dedicated control circuit (500, Fig. 15) for providing a cyclic succession of offset values (c. 11, ll. 29-50; c. 13, ll. 52-67); and a dedicated address circuit (406, Fig. 9) receiving the address of the row read by the read means (c. 3, ll. 39-42) and transmitting to the row driver a new address (c. 3, ll. 31-34).

However, Richards does not teach that the cyclic succession of offset values is provided at a frequency proportional to the display frequency. However, Glennon describes that the cyclic succession of offset values is provided at a frequency proportional to the display frequency (c. 3, ll. 51-65; c. 3, ll. 30-33), as discussed in the rejection for Claim 1.

However, Richards and Glennon do not teach a column driver for activating pixels of the selected line based on the states of memory points. However, Leung teaches a column driver for activating pixels of the selected line based on the states of memory points (c. 2, ll. 2-9, 64-67).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Richards and Glennon to include a column driver for activating pixels of the selected line based on the states of memory points as suggested by Leung because Leung suggests the advantage of not having to write each pixel location, but can write larger blocks of pixel at the same time (c. 1, ll. 35-42; c. 2, ll. 2-9, 64-67).

However, Richards and Glennon do not teach that the new address corresponds to the address of the read row offset by a same pixel position offset value. However, Wu discloses the

new address corresponds to the address of the read row offset by a same pixel position offset value (c. 9, ll. 11-45). This would be obvious for the same reasons given for Claim 1.

24. As per Claim 4, Richards does not teach that the dedicated address circuit is an adder adapted to adding the pixel position offset value to the address of the read row. However, Wu discloses that the dedicated address circuit is an adder adapted to adding the pixel position offset value to the address of read row (c. 9, ll. 11-45). This would be obvious for reasons for Claim 1.

24. As per Claim 5, Richards teaches screen with light-emitting diodes (c. 2, ll. 32-36).

25. Claims 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyachi (US006937224B1) in view of Kuwata (US005754157A).

26. As per Claim 31, Miyachi is relied upon for teachings relative to Claim 30. Miyachi teaches column driver reads image data from first memory (sampling memory) (c. 12, ll. 19-25).

However, Miyachi does not explicitly teach first memory has frame memory that stores image data for entire image to be displayed. However, Kuwata teaches column driver reads image data from first memory (32, Fig. 7), and first memory has a frame memory that stores image data for an entire image to be displayed (c. 13, ll. 53-55; c. 14, ll. 20-45; c. 10, ll. 29-35).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Miyachi so first memory has frame memory that stores image data for entire image because Kuwata teaches this way plurality of scanning lines can be simultaneously selected for driving, which increases speed of driving circuit (c. 1, ll. 62-67; c. 13, ll. 53-55).

27. As per Claim 32, Miyachi teaches that data from the first memory (sampling memory) is stored into the second memory (holding memory) within the column driver (c. 12, ll. 19-25), and the column driver shifts the data (c. 5, ll. 50-58; c. 6, ll. 1-17;c. 3, ll. 46- c. 4, ll. 7).

However, Miyachi does not explicitly teach second memory has register. But, Kuwata teaches data from 1st memory (32, Fig. 7) is stored into second memory (171, Fig. 10) in column driver, and second memory has a register (c. 13, ll. 53-55; c. 14, ll. 20-45; c. 10, ll. 29-57).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify device of Miyachi so second memory has a register as suggested by Kuwata. It is well-known in the art that shift registers are registers in which the data can be shifted. Since Miyachi teaches that the column driver shifts the data, it would be obvious to modify the column driver of Miyachi so that it uses a shift register to shift the data, as suggested by Kuwata.

28. As per Claim 33, Miyachi does not explicitly teach that the register comprises a shift register. However, Kuwata discloses that the register comprises a shift register (171, Fig. 10; c. 10, ll. 48-50). This would be obvious for the same reasons given for Claim 32.

29. Claims 34, 36, and 38-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyachi (US006937224B1) in view of Choi (US 20030076332A1).

30. As per Claim 34, Miyachi is relied on for teachings relative to Claim 30. Miyachi teaches providing a column offset to the second memory (holding memory) (c. 1, ll. 12-20; c. 3, ll. 46-c. 4, ll. 7; c. 5, ll. 50-58; c. 6, ll. 1-7). Miyachi teaches eliminating the afterimage (c. 16, ll. 4-7).

However, Miyachi does not explicitly teach providing column offset direction. However, Choi teaches control circuit (104, Fig. 1) provides column offset direction [0037, 0039].

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Miyachi so that control circuit provides column offset direction as suggested by Choi because Choi suggests that moving the image in different directions is an efficient manner of eliminating the afterimage [0017-0024], and in order to do this, a column

offset direction needs to be provided [0037, 0039]. Since Miyachi teaches a device that eliminates the afterimage, it would be obvious to modify Miyachi with the method taught by Choi, since Choi teaches that this is an efficient way to eliminate the afterimage.

31. As per Claim 36, Miyachi teaches eliminating the afterimage (c. 16, ll. 4-7).

However, Miyachi does not explicitly teach control circuit provides a cyclic succession of column offset values to the second memory. However, Choi discloses that the control circuit provides a cyclic succession of column offset values to the second memory [0036-0040].

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Miyachi so that the control circuit provides a cyclic succession of column offset values to the second memory as suggested by Choi because Choi suggests that this is an efficient way to eliminate the afterimage [0017-0024]. Since Miyachi teaches a device that eliminates the afterimage, it would be obvious to modify Miyachi with the method taught by Choi, since Choi teaches that this is an efficient way to eliminate the afterimage.

32. As per Claim 38, Miyachi teaches shifting storage locations at which the row of image data is stored (c. 4, ll. 4-7).

However, Miyachi does not explicitly teach details of the method for shifting rows, including that control circuit provides row offset value to logic unit; wherein logic unit receives first row address corresponding to row of image data and performs operation on first row address using the row offset value to determine a second row address that is offset from the first row address. However, Choi teaches this limitation, as discussed above in the rejection for Claim 42.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Miyachi to include the method of shifting rows as suggested by Choi because Choi teaches this is needed so that rows are shifted to the correct position [0036, 0041].

33. As per Claim 39, Miyachi does not explicitly teach providing row offset direction. However, Choi teaches control circuit (104) provides row offset direction to logic unit (105, Fig. 1) [0036, 0038]. This would be obvious for the same reasons given in the rejection for Claim 34.

34. As per Claim 40, Miyachi teaches shifting storage locations at which the row of image data is stored (c. 4, ll. 4-7).

However, Miyachi does not explicitly teach details of the method for shifting rows, including that the second row address is determined by adding the row offset value to the first row address or subtracting the row offset value from the first row address. However, Choi teaches this limitation, as discussed above in the rejection for Claim 44. This would be obvious for the same reasons given in the rejection for Claim 38.

35. As per Claim 41, Miyachi does not explicitly teach that the control circuit provides a cyclic succession of row offset values to the logic unit. However, Choi discloses that the control circuit provides a cyclic succession of row offset values to the logic unit [0036-0039]. This would be obvious for the same reasons given in the rejection for Claim 36.

Allowable Subject Matter

36. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on 571-272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH

KEE M. TUNG
SUPERVISORY PATENT EXAMINER